REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 1-4, 6 and 10-33 and 35-40 are all the claims presently pending in the application. Claims 5, 7-9 and 34 have been canceled and claims 1-4, 6, 10-14,17, 18, 31-33, 35 and 37-40 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-2, 4, 6-19, 22-31, 33 and 35-40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Khouja, et al. (U.S. Patent No. 5,682,320). Claims 3, 20 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Khouja, et al., in view of "P1497 Draft Standard for Standard Delay Format", (hereinafter the "SDF publication"), IEEE. Claims 5, 21 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Khouja, et al., in view of Fallah-Tehrani, et al. (U.S. Patent No. 6,405,348).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of analyzing voltage drops on at least one power grid in an integrated circuit chip. The method includes dividing a clock cycle of the integrated circuit chip into a plurality of time periods, performing a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip, and performing at least one simulation of the at least one power grid using extracted power grid information, placement information for the plurality of cells, and the current waveform data to calculate at least one voltage at a plurality of locations within the power grid.

Conventional methods of analyzing voltage drops on a power grid typically assume that all circuits are switching at the same time (Application at page 3, lines 1-5). However, this causes the chip to be over-designed. Other methods simulate functional patterns through the chip logic (Application at page 3, lines 6-16). However, this requires numerous patterns and is, therefore, expensive.

The claimed invention, on the other hand, divides a clock cycle of the chip into a plurality of time periods, and performs a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

II. THE PRIOR ART REFERENCES

A. The Khouja, et al. Reference

The Examiner alleges that Khouja teaches the claimed invention of claims 1-2, 4, 6-19, 22-31 and 35-40. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Khouja.

Khouja discloses a method of computing the power dissipated by a digital circuit using information available at the gate library level. The method estimates the short-circuit power by modeling the energy dissipated by the cell per input transition as a function of the transition time or edge rate, and multiplying that value by the number of transitions per second for that input (Khouja at Abstract).

However, Khouja does not teach or suggest *"performing a static timing analysis to obtain current waveform data for said plurality of time periods for a plurality of cells of said integrated circuit chip"*, as recited in claim 1 and similarly recited in claims 15 and 18.

As noted above, conventional methods of analyzing voltage drops on a power grid typically assume that all circuits are switching at the same time (Application at page 3, lines 1-5). However, this causes the chip to be over-designed. Other methods simulate functional patterns

through the chip logic (Application at page 3, lines 6-16). However, this requires numerous patterns and is, therefore, expensive.

The claimed invention, on the other hand, divides a clock cycle of the chip into a plurality of time periods, and performs a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, Khouja does not teach or suggest these novel features. Indeed, Applicant respectfully submits that the Examiner may be confused by a certain section of Khouja's patent application that deals with a concept that Khouja calls "weighted transition time" (Khouja at col. 11, lines 4-11). Applicants respectfully submit that what Khouja is doing is completely unrelated to the present invention, and is easily distinguishable from the present invention.

In particular, in the Examiner's response to Applicant's arguments, the Examiner stated that "applicant states that Khouja fails to teach or suggest dividing a clock cycle into a plurality of time periods or performing a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period. Interpreted broadly, the weighted transition time is the clock cycle and the transition time of each cell pin is a time period..."

However, Applicant would point out that in Khouja, the weighted transition time is defined at column 11, lines 6-7, where T_{wavg} is given as $T_{wavg} = ((\text{sum}(T_i \times Tr_i)/(\text{sum}Tr_i))$. Thus, by definition, the weighted transition time is less than the transition time for at least one of the cell pins. This implies that "a time period" (by the examiner's interpretation) can be of longer duration than "a clock cycle". Clearly, the Examiner's interpretation is not consistent with the definition of a "clock cycle" in the claimed invention, in which the clock cycle may be divided into "an integer number of time periods" (Application at page 10, line 21-page 11, line 1).

Further, the Khouja definition of weighted transition time is a "per cell" characteristic, whereas the present Application (e.g., Application at page 11, lines 2-18) discusses the assignment of multiple cells to a single time period (or bucket or analysis window). Thus, the

present Application may be considered inconsistent with an interpretation of a time period being derived from the transition time of a single cell.

Further, to those skilled in the art, the definition of "the clock cycle" is well understood to mean the time within which signals propagate from one sequential element to another. This is clearly a distinct concept from a "transition time".

The Examiner further states (e.g., in reference to claim 7 of the present Application) that "Khouja teaches wherein the static timing analysis determines when, where, and the amount of current require for the IC chip..." This is clearly incorrect. In fact, Khouja uses a gate-level netlist with no physical information. Therefore, Khouja does not have access to any physical "where" information.

The Examiner further states "it is noted that the features upon which the applicant relies (i.e., dividing a single, individual clock cycle into "buckets") are not recited in the rejected claim(s)..." This is also clearly incorrect.

Applicant respectfully submits that the Examiner may be confused by the word bucket. Indeed, Applicant notes that the terms "time period", "analysis window" and "bucket" may be considered as meaning the same thing in the present Application. That is, clearly the claims (e.g., claim 1) of the present Application includes a time period or bucket concept.

The Examiner also states that "[i] n reference to claim 11, Khouja teaches wherein static timing analysis comprises assigning a charge used by a circuit to at least one time period, and calculating node voltages for each time period....." This also is clearly incorrect.

Khouja never uses the energy information obtained by his methods to perform a power bus simulation. For example, Khouja never combines his energy values with a physical representation of the design, therefore Khouja can't possibly calculate node voltages. The examiner may be confused by the term "node". Khouja uses this term to refer to a point in a memory model for the integrated circuit. In the present Application, however, the term "node" may be used to refer to a physical location on the integrated circuit.

The Examiner's statements on claims 12-14 are also incorrect. Nowhere in Khouja are any physical parameters investigated. Without physical "where" data, one can't check limits, one

can't back annotate voltages to timing and one can't make a graphical map of the voltages.

Thus, contrary to the Examiner's allegations, Khouja clearly does not teach or suggest dividing a clock cycle of the chip into a plurality of time periods, and performing a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Khouja. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The P1497 DRAFT Standard For Standard Delay Format (SDF) Reference (i.e., the SDF Publication)

The Examiner alleges that the SDF publication would have been combined with Khouja to form the claimed invention of claims 3, 20 and 32. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

The SDF publication discloses a Standard Delay Format (SDF) which is a textual file format for representing the delay and timing information of electronic systems (Draft Standard at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Khouja is directed to a method of computing the power dissipated in a digital circuit, whereas the SDF publication is merely directed to a method of representing and interpreting timing data. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely

states that it would have been obvious to combine the SDF publication with Khouja because the SDF publication "is the standard in the industry".

Moreover, neither the SDF publication, nor Khouja, nor any combination thereof teaches or suggests *"performing a static timing analysis to obtain current waveform data for said plurality of time periods for a plurality of cells of said integrated circuit chip"*, as recited in claim 1 and similarly recited in claims 15 and 18.

As noted above, conventional methods of analyzing voltage drops on a power grid typically assume that all circuits are switching at the same time (Application at page 3, lines 1-5). However, this causes the chip to be over-designed. Other methods simulate functional patterns through the chip logic (Application at page 3, lines 6-16). However, this requires numerous patterns and is, therefore, expensive.

The claimed invention, on the other hand, divides a clock cycle of the chip into a plurality of time periods, and performs a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, the SDF publication does not teach or suggest these novel features. Indeed, Applicant notes that the Examiner does not even allege that the SDF publication teaches this feature.

In fact, the novel features of the claimed invention are not taught or suggested by the SDF publication. Indeed, the Examiner merely attempts to rely on the SDF publication as allegedly suggesting cell characterization data including charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

Indeed, noted above, the SDF publication merely discloses a method of representing and interpreting timing data. Indeed, the SDF publication is completely unrelated to the claimed invention which includes a method of analyzing voltage drops on at least one power grid.

Therefore, the SDF publication does not teach or suggest dividing a clock cycle of the

integrated circuit chip into a plurality of time periods, let alone performing a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip, as in the claimed invention. Therefore, the SDF publication clearly does not make up for the deficiencies of Khouja.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Fallah-Tehrani, et al. Reference

The Examiner alleges that Fallah-Tehrani would have been combined with Khouja to form the claimed invention of claims 5, 21 and 34. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Fallah-Tehrani discloses a method for static timing analysis of deep sub-micron devices in presence of crosstalk. The method attempts to provide an platform for fast and accurate static timing verification of large scale transistor and cell level netlists, with coupled interconnects and high switching speeds. The method also attempts to solve the coupled noise problem in static timing verification.

Specifically, the method attempts to determine worst case aggressor switching time for a cross-coupled interconnect stage. After the worst case aggressor switching time is determined, the netlist is then resimulated using the worst case aggressor switching time to determine more accurate stage delay and slew of the interconnect state. The output waveform is recorded and utilized as the input of subsequent stages (Fallah-Tehrani at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Khouja is directed to a method of computing the power dissipated in a digital circuit, whereas Fallah-Tehrani is merely directed to static timing analysis. Therefore,

these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely states that it would have been obvious to combine Fallah-Tehrani with Khouja because "the effects of crosstalk in static timing analysis can be significant".

However, the Khouja method does not require static timing analysis (e.g., see Khouja at claim 1; col. 103, lines 1-32). In fact, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Fallah-Tehrani, nor Khouja, nor any combination thereof teaches or suggests *"performing a static timing analysis to obtain current waveform data for said plurality of time periods for a plurality of cells of said integrated circuit chip"*, as recited in claim 1 and similarly recited in claims 15 and 18.

As noted above, conventional methods of analyzing voltage drops on a power grid typically assume that all circuits are switching at the same time (Application at page 3, lines 1-5). However, this causes the chip to be over-designed. Other methods simulate functional patterns through the chip logic (Application at page 3, lines 6-16). However, this requires numerous patterns and is, therefore, expensive.

The claimed invention, on the other hand, divides a clock cycle of the chip into a plurality of time periods, and performs a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, the novel features of the claimed invention are not taught or suggested by Fallah-Tehrani. Indeed, the Examiner merely attempts to rely on Fallah-Tehrani as allegedly suggesting

extracting parasitic resistors, capacitors and inductors to generate extracted signal net information which is used to perform said static timing analysis.

In fact, as noted above, the Fallah-Tehrani merely discloses a method of static timing analysis, and is unrelated to the claimed invention which includes a method of analyzing voltage drops on at least one power grid.

In addition, Fallah-Tehrani does not teach or suggest dividing a clock cycle of the integrated circuit chip into a plurality of time periods, let alone performing a static timing analysis to obtain current waveform data for the plurality of time periods for a plurality of cells of the integrated circuit chip, as in the claimed invention. Therefore, Fallah-Tehrani clearly does not make up for the deficiencies of Khouja.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-4, 6 and 10-33 and 35-40, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: 3/15/04

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Brandon Bowers , Group Art Unit # 2825 at fax number (703) 872-9306 this 15th day of March, 2004.

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